Remarks

Claims 1 and 2 are pending herein.

In the Office Action, claim 1 is rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,879,026 to Fukumoto et al. ("Fukumoto"); and claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fukumoto in view of U.S. Patent No. 6,646,289 to Badehi ("Badehi").

In view of the remarks herein, Applicants respectfully request reconsideration and withdrawal of the rejections set forth in the Office Action.

I. Preliminary Matter

In the Office Action Summary, the box indicating that the drawings are objected to by the Examiner is marked. The Office Action itself does not state an objection to the drawings. Applicants' representative, Mary Montebello, contacted Examiner Luu, who advised Ms. Montebello that the box was inadvertently marked. The Examiner faxed Ms. Montebello a corrected Office Action Summary (copy enclosed), wherein the aforementioned box is left unmarked. Applicants wish to thank Examiner Luu for his courtesy and promptness in resolving this matter.

II. Rejection under 35 U.S.C. §102(e)

Claim 1 is rejected under §102(e) as being anticipated by Fukumoto.

Claim 1 is directed to a semiconductor wafer processing method, comprising affixing a protective tape to the front surface of a semiconductor wafer having a plurality of circuits formed on its front surface, grinding the back surface of the semiconductor wafer, and then, subjecting the back surface of the semiconductor wafer to plasma etching. The protective tape is required to have an adhesive layer that is hardened by exposure to ultraviolet radiation. The protective tape is exposed to ultraviolet radiation to harden the adhesive layer **before** the back surface of the semiconductor wafer undergoes plasma etching.

Applicants' claimed invention is designed to overcome the problems produced when the back surface of the semiconductor wafer undergoes plasma etching. After a protective tape is affixed to the front surface of a semiconductor wafer and the back surface of the wafer undergoes

grinding, the front surface of the wafer with the protective tape thereon is placed on a workpiece holding means of a plasma etching apparatus, and the back surface of the wafer undergoes plasma etching treatment. A problem arises, however, wherein the adhesive layer of the protective tape deteriorates due to heating during the plasma etching treatment. Such deterioration causes distortion of the protective tape, which generates a gap between the circuits formed on the front surface of the semiconductor wafer and the protective tape. Plasma etching gas enters this gap and damages the circuit surface. To eliminate this problem, Applicants' claimed invention method calls for using a tape having an adhesive layer that is hardened by exposure to ultraviolet radiation and exposing the protective tape to ultraviolet radiation to harden the adhesive layer before the back surface of the semiconductor wafer undergoes plasma etching. In Applicants' claimed method, exposure of the protective tape to ultraviolet radiation to harden the adhesive layer before the back surface of the wafer undergoes plasma etching prevents the tape from being distorted by heat-induced deterioration during plasma etching. This in turn prevents the formation of a gap between the circuits on the wafer surface and the protective tape, thereby precluding the flow of the plasma etching gas into such a gap.

Fukumoto is cited for disclosing a semiconductor wafer and a method of processing such wafer. According to the Office Action, the patent teaches:

> affixing a protective tape to the front surface of a semiconductor wafer having a plurality of circuits formed on its front surface, grinding the back surface of the semiconductor wafer and then subjecting the back surface of the semiconductor wafer to plasma etching, wherein a tape having an adhesive layer that is hardened by exposure to ultraviolet radiation is used as the protective tape, and ***the protective tape is exposed to ultraviolet radiation to harden the adhesive layer before the back surface of the semiconductor wafer undergoes plasma etching*** (see column 7, lines 50-60; column 8, lines 54-67; column 9, lines 1-5; column 12, lines 49-57; column 14, lines 61-67 and column 15, lines 1-17). [emphasis added]

Applicants respectfully submit that Fukumoto does not teach or suggest that the adhesive or tape be exposed to UV radiation **before** the back surface of the semiconductor wafer undergoes plasma etching.

Fukumoto discloses an adhesive film for protecting the surface of a semiconductor wafer. The adhesive film comprises a substrate film and an adhesive layer formed on one surface of the substrate film (col. 5, lines 21-24). Fukumoto teaches that:

> [t]he adhesive film for protecting the surface of a semiconductor wafer of the present invention is to be used in the non-circuit-formed surface processing of semiconductor wafers wherein the surface where circuits of semiconductor wafers are not formed (hereinafter referred to as "back surface") is processed after adhering the adhesive film for protecting the surface of a semiconductor wafer to the surface where circuits of semiconductor wafers are formed (hereinafter referred to as "front surface") through an adhesive layer generally at around room temperature, that is, around 18 to 30°C. and ***then the adhesive film for protecting the surface of a semiconductor wafer is peeled off by heating*** [emphasis added]. Col. 5, lines 21-36.

Thus, as indicated in the above-quoted passage, Fukumoto teaches that first, the adhesive film is adhered to the semiconductor wafer surface where circuits are formed ("the front surface"), then the semiconductor wafer surface wherein circuits are not formed ("the back surface") is processed, after which the adhesive film is peeled off by heating. The patent teaches that the back surface processing of the wafer is characterized by using the adhesive film in conducting a grinding process, a chemical etching process or both a grinding process and a chemical etching process at the same time, against the non-circuit-formed surface of the wafer (col. 16, lines 19-24). Fukumoto teaches that:

> More specifically, at around 18 to 30°C. in general, the peeling film is peeled off from the above adhesive film to expose the surface of the adhesive layer, said adhesive film being adhered to on the surface of the semiconductor wafer through the adhesive layer. The semiconductor wafer is next fixed to a chuck table of grinding machine or so on through the substrate film layer of the adhesive film, conducting grinding process, chemical etching process and so on against the back surface of semiconductor wafers. Col. 16, lines 24-34.
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> Chemical etching process is exemplified by chemical solution treatment, method of conducting chemical etching and back grinding denominated as CMP at the same time, ***plasma etching*** and so on [emphasis added]. Col. 17, lines 16-19.

> ***After completion of [the] back grinding process, chemical solution treatment and so on*** of [the] wafers, the adhesive film is peeled off from the surface of [the] wafers [emphasis added]. Col. 17, lines 31-33. See also col. 16, lines 41-42.

Although Fukumoto enumerates plasma etching as an example of the processing method to which the back surface of the wafer is subjected, Fukumoto does not describe the problems caused by plasma etching, which Applicants discussed hereinabove.

Fukumoto teaches that if the adhesive layer contains a radiation curing adhesive agent, the adhesive agent can be "cured by irradiating radiation such as ultra-violet wave before peeling the adhesive film from the surface of semiconductor wafers to decrease the adhesive strength" (col. 15, lines 22-25). That is, in Fukumoto, the adhesive layer is exposed to UV radiation to facilitate the peeling off of the adhesive film from the semiconductor wafer surface. This is the only instance disclosed in Fukumoto where the adhesive layer is exposed to UV radiation. Such exposure to UV radiation occurs **after** the back surface processing (i.e., after the chemical etching process (which can be plasma etching)) of the wafer. Fukumoto does not teach or suggest exposing the adhesive layer to UV radiation **before** the chemical etching of the wafer.

Thus, for at least this reason, Applicants submit that Fukumoto does not anticipate instant claim 1.

III. Rejection under 35 U.S.C. §103(a)

Claim 2 is rejected under §103(a) as being unpatentable over Fukumoto in view of Badehi.

Claim 2 is directed to a semiconductor wafer processing method, comprising forming dividing grooves having a predetermined depth along a plurality of streets on the front surface of a semiconductor wafer having a plurality of streets on the front surface in a lattice form and a circuit formed in each of a plurality of areas sectioned by the plurality of streets, affixing a protective tape to the front surface of a semiconductor wafer having the dividing grooves formed thereon, grinding the back surface of the semiconductor wafer until the dividing grooves are exposed to separate into individual circuits, and then, executing plasma etching of the back surface of the semiconductor wafer. As in claim 1, the protective tape used in claim 2 is a tape

having an adhesive layer that is hardened by exposure to ultraviolet radiation. Also as in claim 1, the protective tape in claim 2 is exposed to ultraviolet radiation to harden the adhesive layer **before** the back surface of the semiconductor wafer undergoes plasma etching.

According to the Office Action, Fukumoto teaches the features of claim 2 except for the formation of dividing grooves having a predetermined depth along a plurality of streets on the front surface of the semiconductor wafer, the plurality of streets being in a lattice form, and a circuit formed in each of a plurality of areas sectioned by the plurality of streets. Badehi is cited for teaching an integrated circuit, the formation of dividing grooves having a predetermined depth along a plurality of streets on the front surface of a semiconductor wafer, the plurality of streets on the front surface being in a lattice form, a circuit formed in each of a plurality of areas sectioned by the plurality of streets, and the affixing of a protective tape to the front surface of the wafer having the dividing grooves formed thereon (see Figs. 1A-1C). According to the Examiner, it would have been obvious to have modified the semiconductor wafer taught in Fukumoto to include the aforementioned features disclosed in Badehi.

Like Fukumoto, Badehi does not teach or suggest exposing an adhesive layer affixed to a semiconductor wafer to UV radiation **before** the chemical etching of the wafer. Therefore, for at least this reason, Fukumoto in view of Badehi would not have rendered instant claim 2 obvious.

IV. Conclusion

In view of the remarks herein, Applicants respectfully request that the rejections set forth in the Office Action be withdrawn and that claims 1 and 2 be allowed.

As noted above, this Request for Reconsideration is being filed with a Petition for Extension of Time (One-Month) and a check for the sum of $120 for the required extension fee. If any additional fees under 37 C. F. R. §§ 1.16 or 1.17 are due in connection with this filing, please charge the fees to Deposit Account No. 02-4300, Order No. 033773.064.

Respectfully submitted,

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Enclosures: (1) Petition for Extension of Time (One-Month)
(2) Check for the sum of $120
(3) Copy of Corrected Office Action Summary